WE CLAIM

Sub B1

1. A method of displaying digital video data comprising pixel values using pulse width modulation, comprising the steps of:

offsetting a first said pixel value a first predetermined amount to form a first offset pixel value and displaying said first offset pixel value during a first display frame; and

offsetting said first said pixel value by the opposite of said first predetermined amount to form a second offset pixel value and displaying said second offset pixel value during a second display frame, such that the average of said displayed first offset pixel value and said second offset pixel value is said first pixel value.

2. The method as specified in Claim 1 wherein the value of said first predetermined amount is selected as a function of said first pixel value.

3. The method as specified in Claim 1 wherein said first offset pixel value is greater than or less than said first pixel value as a function of the spatial location that said first pixel value is to be displayed.

4. The method as specified in Claim 1 wherein said pixel values are displayed using a plurality of weighted bit-planes, wherein said first pixel values close to a bit transition of said bit-planes are offset during said first display frame and said second display frame.

5. The method as specified in Claim 1 wherein said first display frame and said second display frame are consecutive.

6. A system of displaying digital video data comprising pixel values using pulse width modulation, comprising:

a logic circuit offsetting a first said pixel value a first predetermined amount to form a first offset pixel value said logic circuit also offsetting said first said pixel value by the opposite of said first predetermined amount to form a second offset pixel value; and

display means displaying said first offset pixel value during a first display frame and displaying said second offset pixel value during a second display frame, such that the average of said displayed first offset pixel value and said second offset pixel value is said first pixel value.

7. The system as specified in Claim 6 wherein the value of said first predetermined amount is selected by said logic circuit as a function of said first pixel value.

8. The system as specified in Claim 6 wherein said first offset pixel value is greater than or less than said first pixel value as a function of the spatial location that said first pixel value is to be displayed.

9. The system as specified in Claim 6 wherein said pixel values are displayed using a plurality of weighted bit-planes, wherein said first pixel values close to a bit transition of said bit-planes are offset during said first display frame and said second display frame.

10. The system as specified in Claim 6 wherein said first display frame and said second display frame are consecutive.